UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,519	08/18/2003	Naoki Kuwata	122.1561	1583

21171 7590 07/20/2009
STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
JOSEPH, JAISON	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
07/20/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Arguments

Applicant's arguments filed 6/25/2009 have been fully considered but they are not persuasive.

Applicant argue, "*Claims 1,2, and 3 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The final Office Action, in particular, asserts that the recitation "by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence," is not described in the specification. The rejection is traversed."* However the Office respectfully disagrees. Office respect fully submits that figure 6 and 7 disclose the prior art and is inn the background of the invention section. Further Figure 10 discloses the control circuit is controlling the phase lock signal based on the output of both phase comparators 45 and 46. further nowhere in the present specification disclose control circuit controlling "***by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence*** ". Applicant alleges that the present specification teaches said limitation (see the remarks). However does not show where in the present specification said limitation is disclosed. Clarification is required. Thus the claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For the purpose of the art rejection, Examiner consider the claims without the limitation "...by using phase information on a data signal which is not used by said phase comparator circuit before detecting said absence...".

Applicant further argue "*Neither the section of the subject application entitled "Background Art" nor Soda, on the other hand, teach, disclose, or suggest a "timing extraction circuit which uses a Phase Locked Loop (PLL) circuit containing a phase comparator circuit performing a phase comparison, by using a part of phase information on a data signal between a data signal of bit rate B (bits/s) and a clock signal of B/2 (Hz) at intervals of 2/B (sec)," as recited in claim 1".* The office respectfully disagrees. the office submits that the phase comparator circuit described in the background art (Applicant admitted prior art) and in the present invention are exactly the same (see figure 3 and figure 10). Only the output of the phase comparator is used for detector circuit and controlling circuit (see figure 10). Therefore AAPA teach said limitation. Examiner further submits that the rejection is made based on obviousness not anticipation. Furthermore, Applicant is reminded that Examiner is entitled to give broadest reasonable interpretation to the language of the claims.

Further AAPA discloses a timing extraction circuit which uses a PLL circuit containing a phase comparator circuit for performing a phase comparison between a data signal of bit rate B ad a clock signal of B/2 at intervals of 2/B (see figure 3), AAPA does not disclose the timing extraction circuit further comprise a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization. In analogous art, Soda teaches a PLL circuit comprising a detection circuit for detecting the absence of an output of phase comparison information

from said phase comparator circuit by receiving a data signal of prescribed pattern before the occurrence of a loss of synchronization at the Phase locked loop (see figure 2, component 23 and column 4, line 14 – 33); and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization (see figure 2, component 23 and column 4, line 14 – 33) [Applicant admits that when the PLL circuit receives a prescribed pattern, the PLL will run out of synchronization (i.e. if the prescribed pattern is detected (absence of the comparison output), it will indicate the possible collapse of the synchronization). Soda teaches a detector detecting the collapse of the synchronization from the output of the phase comparator is equivalent to detecting the prescribed pattern (absence of the comparison output).].). Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to incorporate the Soda's PLL control circuit in AAPA to have a phase locking loop circuit which need not have an adjusting terminal for use in adjusting the frequency range. Therefore AAPA in view of Soda teach all cited limitations thus the Office maintains the rejection of claim 1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAISON JOSEPH whose telephone number is (571)272-6041. The examiner can normally be reached on M-F 9:30 - 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. J./
Examiner, Art Unit 2611

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611